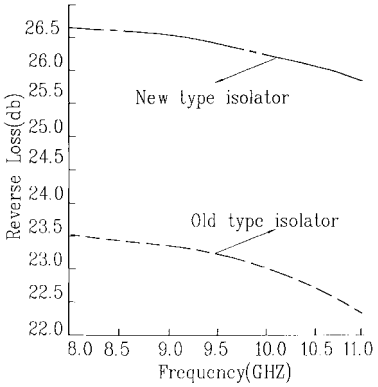


Fig. 4. Calculated reverse loss with frequency for new type isolator and old type isolator in $X$-band.

considered. The propagation constant transcendental equation has been deduced. By using appropriate ridged waveguide instead of rectangular one, it is possible to increase the isolation and bandwidth of the field displacement isolator, thus making it easier to get a good match. However, the forward insert loss of the new type device is slightly larger than that of the old type devise, and how to reduce the forward loss is of further work. The authors believe that this paper has resulted in a sufficient amount of knowledge regarding the device and provides a quantitative guide to the design of microwave devices.

## REFERENCES

[1] T. S. Chen, "Nonreciprocal attenuation of ferrite in single ridge waveguide," *IRE Trans. Microwave Theory Tech.*, vol. MTT-48, pp. 247–248, May 1960.
[2] W. Junding, "Analysis of transverse magnetization phase shifter of cross waveguide," in *Nat. Interchange Conf. Magnetic Material, Device Tech.*, Guanxian, Sichuan, China, Oct. 1977, pp. 1–8.
[3] ——, "Experimental studies of latching ferrite phase shifter of back ridged waveguide," *Acta. Electron. Sin.*, no. 3, pp. 44–51, Sept. 1979.
[4] W. Junding, Y. Z. Xiong, M. J. Shi, G. F. Cheng, and M. D. Zu, "Analysis of twin ferrite toroidal phase shifter in grooved waveguide," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 616–621, Apr. 1994.
[5] Y. S. Xu, "Microwave ferrite toroidal phase shifter in grooved waveguide with reduced sizes," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1095–1097, June 1988.
[6] A. Mizobuchi and W. Kwrebagashi, "Nonreciprocal remanence ferrite phase shifter using the grooved waveguide," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 1012–1017, Dec. 1978.
[7] R. L. Comstock and C. E. Fay, "Operation of the field displacement isolator in rectangular waveguide," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-8, pp. 605–611, Nov. 1960.
[8] I. R. Whinery and H. W. Jamieson, *Proc. IRE*, vol. 32, pp. 98–115, Feb. 1944.

# An Accurately Scaled Small-Signal Model for Interdigitated Power P-HEMT up to 50 GHz

Shen-Whan Chen, Olaleye Aina, Weiqi Li, Lee Phelps, and Tim Lee

***Abstract*—In this paper, the authors report an approach for constructing scalable small-signal models for interdigitated power pseudomorphic high-electron-mobility transistors (P-HEMT's). By using cold-FET and Yang–Long measurement, as well as direct extraction procedures, scaling rules for extrinsic components were established that allow accurate models over a broad frequency range. These models have been used to design ultrawide-band monolithic microwave integrated circuits (MMIC's) up to 50 GHz.**

## I. INTRODUCTION

Small-signal equivalent models are used frequently in the design of power amplifier (PA), low-noise amplifier (LNA), and other subsystem components. A small-signal model which provides good accuracy and can be scaled based on layout structures, as well as gatewidth, is useful when various FET sizes are needed or models are simply not available. Unlike the small-signal model that is determined by computer optimization, a physically related one can be useful in the characterization of fabrication processes and for scaling purposes. In addition to providing an equivalent circuit to predict MMIC electrical performance, a scalable modeling approach is also useful in determining the noise parameters [1]–[2]. In this paper, an approach to constructing a scalable small-signal model from cold-FET, Yang–Long measurement, and RF data for an interdigitated power pseudomorphic high-electron-mobility transistor (P-HEMT) is presented. Approaches for selecting the parameters from data sets are discussed. The scaling factors for extrinsic components ($R_g$, $R_d$, $R_s$, $L_g$, $L_d$, $L_s$, $C_{\rm pg}$, and $C_{\rm pd}$) are given after careful examination of the measured data. The $S$-parameter comparison between scaled models and measured data are shown up to 50 GHz.

## II. POWER P-HEMT DEVICE STRUCTURE AND EQUIVALENT CIRCUIT

The pseudomorphic InGaAs/AlGaAs HEMT device structure was used in this paper. The device profile is a double-heterojunction HEMT grown by molecular beam epitaxy (MBE). Silicon planar doping is employed on both heterojunctions to provide carriers to the InGaAs channel. The AlGaAs layer with the planar doping was left undoped and the Schottky gate was recessed to this region. Ohmic contacts were formed with an optimized rapid thermal annealing (RTA) AuGeNi-based metallization scheme. Device isolation was achieved by boron ion implantation. The devices were passivated with SiN film deposited by plasma-enhanced chemical-vapor deposition (PECVD). Due to the use of undoped AlGaAs, the gate–drain breakdown voltage (defined at 1 mA/mm) is greater than 12 V.

Fig. 1 shows the chosen equivalent circuit topology for the interdigitated power P-HEMT. The P-HEMT layout in wafer process control monitored (PCM) sites is shown in Fig. 2. The $S$-parameters of five different FET's, 100 $\mu$m (25 $\times$ 4, two gate feeds), 198 $\mu$m (33 $\times$ 6, three gate feeds), 300 $\mu$m (30 $\times$ 10, five gate feeds), 396 $\mu$m (33 $\times$ 12, six gate feeds), and 600 $\mu$m (50 $\times$ 12, six gate feeds) are measured and their small-signal models are extracted with methods discussed below.

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The authors are with the M/A-COM, IC Business Unit, Millimeter IC Product, Clarksburg, MD 20871 USA.

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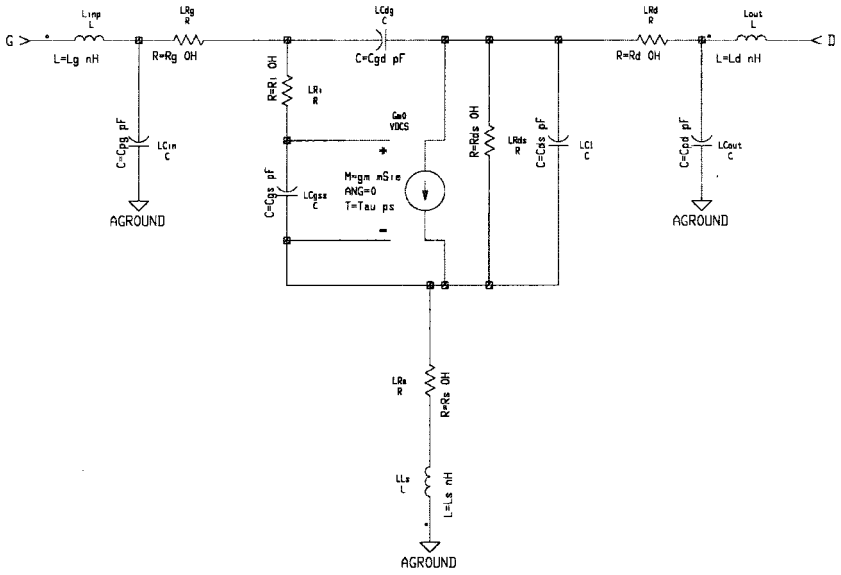


Fig. 1. Equivalent circuit of interdigitated power P-HEMT.

## III. Extraction of Parameters

The following equations [3], [4], [6] were used to calculate model parameters:

$$\mathrm{Im}\,(Y_{11}) = j\,w(C_{\mathrm{pg}} + \tfrac{2}{3}\,C_b) \tag{1}$$

$$\mathrm{Im}\,(Y_{12}) = \mathrm{Im}\,(Y_{21}) = -j\,w\left(\frac{C_b}{3}\right) \tag{2}$$

$$\mathrm{Im}\,(Y_{22}) = j\,w(C_{\mathrm{pd}} + \tfrac{2}{3}\,C_b) \tag{3}$$

where $C_b$ is the fringing capacitance due to the depleted layer extension at each side of the gate.

$$Z_{11} = R_s + R_g + \frac{R_c}{3} + \frac{nkT}{qI_g} + jw(L_s + L_g) \tag{4}$$

$$Z_{12} = Z_{21} = R_s + \frac{R_c}{2} + jwL_s \tag{5}$$

$$Z_{22} = R_s + R_d + R_c + jw(L_s + L_d) \tag{6}$$

where $R_c$ is the channel resistance, $n$ is the ideality factor, $k$ is the Boltzmann constant ($1.380\,54e-23J^{\circ}\mathrm{K}^{-1}$), $q$ (1.6021e-19 C) is the electron charge, and $T$ is the ambient temperature in Kelvin.

$$C_{\mathrm{gd}} = -\frac{\mathrm{Im}\,(Y_{12})}{w} \tag{7}$$

$$C_{\mathrm{gs}} = \frac{\mathrm{Im}\,(Y_{11}) - wC_{\mathrm{gd}}}{w}\left\{1 + \frac{[\mathrm{Re}\,(Y_{11})]^2}{[\mathrm{Im}\,(Y_{11}) - wC_{\mathrm{gd}}]^2}\right\} \tag{8}$$

$$R_i = \frac{\mathrm{Re}\,(Y_{11})}{[\mathrm{Im}\,(Y_{11}) - wC_{\mathrm{gd}}]^2 + [\mathrm{Re}\,(Y_{11})]^2} \tag{9}$$

$$g_m = \sqrt{\{[\mathrm{Re}\,(Y_{21})]^2 + [\mathrm{Im}\,(Y_{21}) + wC_{\mathrm{gd}}]^2\}} \times \sqrt{(1 + w^2C_{\mathrm{gs}}^2R_i^2)} \tag{10}$$

$$\tau = \frac{1}{w}\,\arcsin\left[\frac{-wC_{\mathrm{gd}} - \mathrm{Im}\,(Y_{21}) - wC_{\mathrm{gs}}R_i\,\mathrm{Re}\,(Y_{21})}{g_m}\right] \tag{11}$$

$$C_{\mathrm{ds}} = \frac{\mathrm{Im}\,(Y_{22}) - wC_{\mathrm{gd}}}{w} \tag{12}$$

$$g_{\mathrm{ds}} = \mathrm{Re}\,(Y_{22}). \tag{13}$$

All the $S$-parameter measurements are done with line-reflected reflected-match (LRRM) off-wafer calibration and data were taken from 0.5 to 50 GHz. Based on (1)–(3), the extrinsic capacitance were extracted from the cold-FET measurements ($V_d = 0$) at pinchoff condition [3]. The extracted value of $C_{\mathrm{pg}}$ and $C_{\mathrm{pd}}$ usually do not vary much throughout the frequency band and they were chosen at the middle frequency ($\approx$ 25 GHz). Table I shows the extracted values of the average capacitance for FET's.

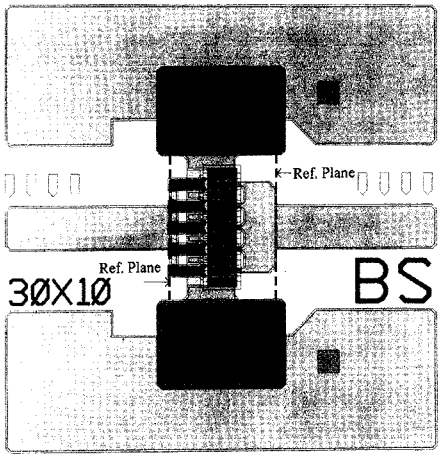


Fig. 2. Layout of the interdigitated power P-HEMT.

TABLE I
The Values of Average Extrinsic Capacitance (pF) Measured at Pinchoff Condition

| 100 um | | 198 um | | 300 um | | 396 um | | 600 um | |
|---|---|---|---|---|---|---|---|---|---|
| Cpg | Cpd | Cpg | Cpd | Cpg | Cpd | Cpg | Cpd | Cpg | Cpd |
| 0.016 | 0.014 | 0.024 | 0.011 | 0.034 | 0.004 | 0.044 | 0.006 | 0.039 | 0.005 |

In order to extract the extrinsic resistance and inductance, cold-FET $S$-parameter measurements were done at forward bias condition ($V_g > 0.7$ V). Theoretically, larger gate current should deliver better accuracy. However, excessive gate current would damage the device. After numerous tests, a gate current density of 150 mA/mm was determined to be very much sufficient. Equations (4)–(6) were used to compute $R_s$, $R_d$, $R_g$, $L_s$, $L_d$, and $L_g$ [4]. The above equations provide only five equations with six unknowns. Therefore, the Yang–Long three-terminal dc method [5] for $R_d$ is used to provide the necessary additional equation.

The extracted value of extrinsic inductors also do not vary much throughout the frequency band and their values were chosen from the

TABLE II
THE VALUES OF AVERAGE EXTRINSIC RESISTANCE AND INDUCTANCE (nH) MEASURED AT FORWARD BIAS CONDITION

| | Rd | Rs | Rg | Ld | Ls | Lg |
|---|---|---|---|---|---|---|
| 100 um | 4.1 | 4.6 | 5.1 | 0.023 | 0.002 | 0.017 |
| 198 um | 2.1 | 2.3 | 3.5 | 0.025 | 0.003 | 0.016 |
| 300 um | 1.3 | 1.6 | 2.2 | 0.031 | 0.005 | 0.018 |
| 396 um | 1.0 | 1.2 | 1.9 | 0.018 | 0.005 | 0.014 |
| 600 um | 0.6 | 0.9 | 2.0 | 0.021 | 0.005 | 0.010 |

TABLE III
THE VALUES OF INTRINSIC COMPONENTS MEASURED AT 50% $I_{\rm dss}$

| | Cgd (pF) | Cgs (pF) | Cds (pF) | Ri | Rds | gm (mS) | Tau (pS) |
|---|---|---|---|---|---|---|---|
| 100 um | 0.0064 | 0.1022 | 0.0189 | 6.7 | 775 | 28.7 | 1.78 |
| 198 um | 0.0106 | 0.1998 | 0.0391 | 3.9 | 396 | 54.7 | 1.50 |
| 300 um | 0.0160 | 0.3200 | 0.0640 | 2.7 | 270 | 79.0 | 1.43 |
| 396 um | 0.0190 | 0.3790 | 0.0770 | 2.0 | 206 | 97.0 | 1.36 |
| 600 um | 0.0260 | 0.6050 | 0.1110 | 1.5 | 137 | 138.0 | 1.33 |

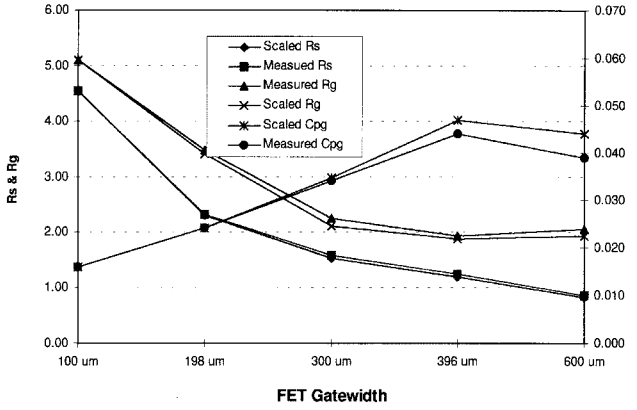


Fig. 3. Comparison between measured and scaled $R_s$, $R_g$, and $C_{\rm pg}$.

middle frequency. Regarding the resistors, their extracted values are accurate only at low frequencies. The resistor values were chosen at 1 GHz or below. Table II shows the measured results of the average inductance and resistance. Due to the use of ground–signal–ground (G–S–G) wafer probes which have very little current would flow through the via holes, and would result in a very small $L_s$.

A direct extraction method [6], corresponding to (7)–(13) was used to compute the intrinsic components, and their value was chosen from the middle frequency. Since the component values of $R_{\rm ds}$ and $R_i$ are sensitive to the calibration errors as well as the probe's touch-down position, poor $S$-parameter measurements could result in negative value. However, this problem can be resolved by curve fitting $S_{11}$ and $S_{22}$ for realistic values of $R_i$, and $R_{\rm ds}$, respectively. Table III shows these intrinsic components for various FET sizes.

## IV. DETERMINATION OF THE SCALING FACTORS

The value of extrinsic capacitors $C_{\rm pg}$ and $C_{\rm pd}$ are related to the gate feeds and drain pad, respectively. The scaling function for these parameters is complicated due to the occurrence of higher order modes within these regions. However, an empirically determined scaling rule can be applied for $C_{\rm pg}$

$$\frac{C^1_{\rm pg}}{C^2_{\rm pg}} = \left(\frac{N^1_{\rm GF}}{N^2_{\rm GF}}\right)\left(\frac{S^2_{\rm cpw}}{S^1_{\rm cpw}}\right)^{0.38} \tag{14}$$

where $N_{\rm GF}$ is the total number of gate feeds and $S_{\rm cpw}$ is the spacing distance of the inner coplanar waveguide (CPW) transmission line. Fig. 3 shows the comparison between measured and scaled $C_{\rm pg}$.

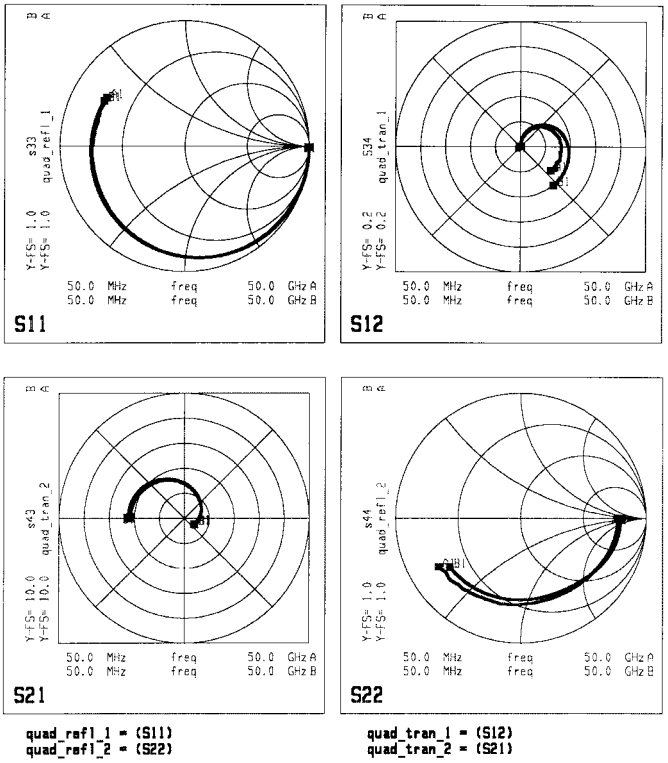


Fig. 4. Comparison between measured and scaled 198-$\mu$m device.

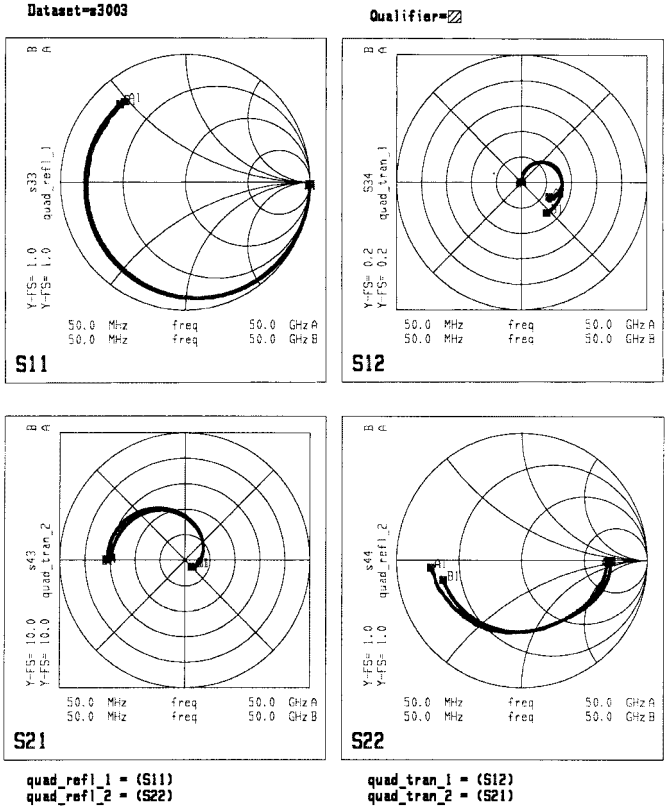


Fig. 5. Comparison between measured and scaled 300-$\mu$m device.

Although the drain pad has a larger area as compared with the gate feeds, the capacitance of $C_{\rm pd}$ is actually smaller. The role of this drain

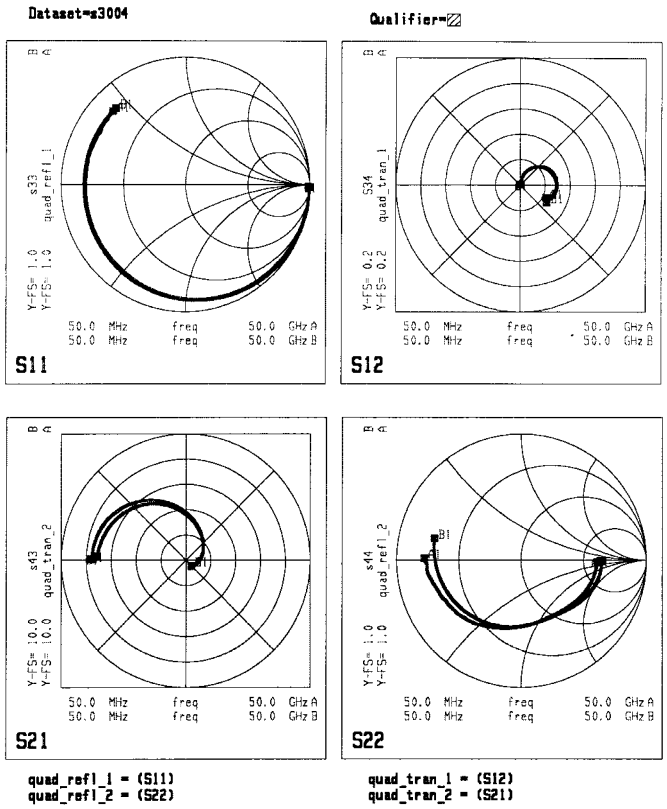


Fig. 6. Comparison between measured and scaled 396-$\mu$m device.

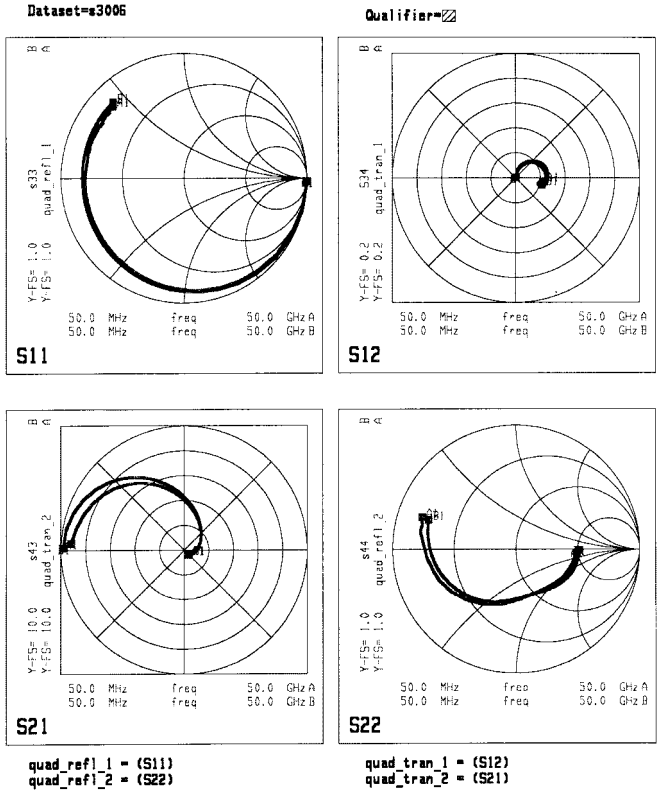


Fig. 7. Comparison between measured and scaled 600-$\mu$m device.

pad is not acting as a capacitor plate but introducing discontinuity within the transmission line system, which causes more magnetic energy to be generated in the higher order modes. Since the value of $C_{\rm pd}$ is usually around, or less than, tens of picofarad, its effect on overall performance is insignificant. Scaling is really not necessary for this capacitor. However, if scaling is used, it should be inversely proportional to the size of the drain pad.

From Table II, it can be seen that the values of extrinsic inductors $L_g$, $L_d$, and $L_s$ do not vary much and they do not need any scaling. But the extrinsic resistors do need to be scaled. After carefully examining the measured data, the scaling formula was determined to be as follows:

$$\frac{R_d^1}{R_d^2} = \frac{R_{\rm s}^1}{R_{\rm s}^2} = \frac{W_{\rm g}^2}{W_{\rm g}^1} \tag{15}$$

$$\frac{R_{\rm g}^1}{R_{\rm g}^2} = \frac{W_{\rm g}^2}{W_{\rm g}^1}\,\frac{L_{\rm gf}^1}{L_{\rm gf}^2} \tag{16}$$

where $W_{\rm g}$ is the gate width and $L_{\rm gf}$ is the length of gate finger. Fig. 6 shows the comparison between measured and scaled $R_{\rm s}$ and $R_{\rm g}$.

For the intrinsic components, the scaling rule is simple and conventional and is either proportional or inversely proportional to the gate width.

Five different gate widths, 100-$\mu$m, 198-$\mu$m, 300-$\mu$m, 396-$\mu$m, and 600-$\mu$m power P-HEMT were used in this work. The $S$-parameters at 5-V drain voltage and 50% $I_{\rm dss}$ were carefully measured and the small-signal models were extracted, respectively. Figs. 4–7 shows good agreement in $S$-parameters between the measured and the scaled models determined by using the scaling rules.

## V. Conclusion

An extraction approach for determining the small-signal model of an interdigitated power P-HEMT device was described. From the measured data, new scaling rules have been determined for extrinsic components. The results in this paper show that accurate models can be generated up to 50 GHz by using this approach.

## References

[1] M. W. Pospieszalski, "Modeling of noise parameters of MESFET's and MODFET's and their frequency and temperature dependence," *IEEE Trans. Microwave Theory Tech.*, vol. 37, pp. 1340–1350, Sept. 1989.

[2] B. Hughes and H. Kondoh, "12-GHz low-noise MMIC amplifier designed with a noise model that scales with MODFET size and bias," *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 2311–2316, Dec. 1993.

[3] P. M. White and R. M. Healy, "Improved equivalent circuit for determination of MESFET and HEMT parasitic capacitances from 'Coldfet' m measurements," *IEEE Microwave Guided Wave Lett.*, pp. 453–454, Dec. 1993.

[4] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1159, July 1988.

[5] L. Yang and S. I. Long, "New method to measure the source and drain resistance of the GaAs MESFET," *IEEE Electron Device Lett.*, vol. EDL-7, p. 75–77, Feb. 1986.

[6] M. Berroth and R. Bosh, "Broad-band determination of the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 891–895, July 1990.